UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/732,998	12/11/2003	Michael DeMar Taylor	DATUMTE.015A	8286

20995 7590 05/22/2006

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
PATEL, HETUL B	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/732,998	TAYLOR ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) *28-35* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to communication filed on May 08, 2006. This response has been entered and carefully considered. Claims 22-35 have been newly added; and claims 1, 3, 8-9, 14-15 and 20 have been amended. Therefore, claims 1-35 are currently pending in this application.

2. Applicant's arguments filed on May 08, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Election/Restrictions

3. Newly submitted claims 28-35 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Inventions of each of the newly presented independent claims 28-35 are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, each of the newly presented independent claims 28-35 has separate utility such as using the system controller device claimed in newly presented independent claims 28-35 with a microprocessor different from the microprocessor as claimed in original claims 1-21. See MPEP § 806.05(d).

4. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 28-35 are withdrawn from consideration

as being directed to a non-elected invention. Newly added claims 22-27 are examined as they directed to an elected invention, i.e. further limit the original claims 1-21. See 37 CFR 1.142(b) and MPEP § 821.03.

Claim Objections

5. Claims 1 and 22 are objected to because of the following informalities:

The phrase should be stated as "retrieving, into the microprocessor, a cache tag ..." instead of "retrieving into the microprocessor a cache tag ..." as disclosed in the claim 1.

The phrase should be stated as "... the microprocessor is configured to ..." instead of "... the microprocessor in configured to ..." as disclosed in the claim 22.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-12 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the 'Background of Invention' section of this application, hereinafter, BOI in view of Feierbach et al. (USPN: 6,065,097) hereinafter, Feierbach further in view of Chen (USPN: 5,752,045).

As per claim 1, BOI teaches a method of processing a memory read request from a central processing unit (CPU) of a microprocessor, the method comprising: retrieving a cache tag associated with the memory read request from a cache memory bank (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) that is external to the microprocessor, wherein the cache memory bank stores cache tags and cache data in separate memory locations; external to the microprocessor, comparing the cache tag to a memory address associated with the memory read request to assess whether data requested by the CPU resides within the cache memory bank (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

However BOI does not teach (i) the cache tag is retrieved into the microprocessor, and (ii) the comparison of the cache tag with the memory address occurs within the microprocessor. Feierbach, on the other hand, teaches that the microprocessor (i.e. the CPU 52 in Fig. 2) performs the tag comparison (e.g. see Col. 4, line 56-59 and Fig. 2). Therefore, the comparison of the cache tag with the memory address occurs within the microprocessor and in order to do that the cache tag has to be retrieved into the microprocessor as claimed. Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teachings of Feierbach in the method taught by BOI so any RAM memory can be used as a tag RAM. In doing so, the user can upgrade the system by replacing the tag RAM with the general purpose RAM without having the built-in comparison circuitry. Therefore, it would be cheaper to expand the tag RAM space.

Neither BOI nor Feierbach teaches the further limitation of subsequent to retrieving the cache tag into the microprocessor, the cache data is retrieved into the microprocessor from the cache memory bank, whereby the retrieval of the cache data into the microprocessor does not overlap in time with the retrieval of the cache tag into the microprocessor. Chen, on the other hand, teaches that first the address issued by the CPU (10 in Fig. 2) is compared with the tag address stored in the tag RAM (i.e. 30 in Fig. 2); and then if the result of the comparison is a cache hit, then the corresponding data is accessed from the data SRAM (i.e. 20 in Fig. 2) (e.g. see Figs. 2 and 4 and Col. 2, lines 18-34), in other words, the cache data is retrieved subsequent to retrieving the cache tag and these two retrieval processes do not overlap in time as claimed. Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teachings of Chen in the method taught by the combination of BOI and Feierbach. In doing so, the data is retrieved from the data cache only if it exists in the data cache otherwise from the main memory. Therefore, the data traffic on the cache data/address bus is reduced by not receiving the wrong data. Therefore, the power saving and the performance of the system increases. Although Chen is not retrieving the cache tag in the microprocessor, it would have been obvious to retrieve it and compare it with the memory address requested by the microprocessor inside the microprocessor as taught by Feierbach for the benefits listed above.

As per claim 3, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above and furthermore, Feierbach teaches that the cache tag

and the cache data are retrieved in sequence from the cache memory bank (i.e. 58 in Fig. 2) over common set of bus lines (i.e. 56 in Fig. 2 and set of bus lines made with combination of tag and data lines shown in Fig. 3; a single unified memory bus as disclosed in the Abstract) that connects the microprocessor (i.e. 52 in Fig. 2) to the cache memory bank (i.e. 58 in Fig. 2) (e.g. see Fig. 2).

As per claim 4, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that comparing the cache tag to the memory address within a system controller device that interfaces the microprocessor to a main memory (e.g. see Fig. 4).

As per claim 5, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above and furthermore, BOI teaches that the comparison circuitry identifies whether the memory address supplied by the microprocessor matches the data resident in the level 2 cache, which is similar to mapping the memory address, supplied by the microprocessor, into a cache tag address and a cache data address that are sequentially provided to the cache memory bank to retrieve the cache tag and the cache data therefrom (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

As per claim 6, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above and furthermore, BOI teaches that mapping the memory address comprises using an address mapping function that subdivides a memory space of the cache memory bank into separate cache tag locations and cache data locations (i.e. cache data are stored in the Level 2 cache data element in separate locations from the cache tags in the Level 2 cache tag element) (e.g. see Fig. 4).

As per claim 7, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above. The further limitation of, having an address transformation circuit that converts the memory address into cache memory addresses for reading the cache tag and cache data, in inherently embedded in the microprocessor taught by BOI. The Fig. 4 of BOI clearly shows that the microprocessor provides the cache index (i.e. the cache memory address) to the cache data and tag memories (e.g. see Fig. 4). Therefore, there has to be an address transformation circuit present in the microprocessor taught by BOI to convert the memory address into the cache index (i.e. the cache memory address) for reading the cache tag and cache data from the cache memory bank.

As per claim 8, BOI teaches a microprocessor system, comprising a bank (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) of general purpose random access memory that stores both cache tags and cache data in separate memory locations; and a microprocessor connected to the bank of general purpose random access memory, and configured to use the bank of general purpose random access memory as an external cache memory (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4).

However BOI does not teach (i) the cache tag is retrieved into the microprocessor, and (ii) the comparison of the cache tag with the memory address occurs within the microprocessor. Feierbach, on the other hand, teaches that the microprocessor (i.e. the CPU 52 in Fig. 2) performs the tag comparison (e.g. see Col. 4, line 56-59 and Fig. 2). Therefore, the comparison of the cache tag with the memory

address occurs within the microprocessor and in order to do that the cache tag has to be retrieved into the microprocessor as claimed. Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teachings of Feierbach in the method taught by BOI so any RAM memory can be used as a tag RAM. In doing so, the user can upgrade the system by replacing the tag RAM with the general purpose RAM without having the built-in comparison circuitry. Therefore, it would be cheaper to expand the tag RAM space. Furthermore, Feierbach teaches that the cache tag and the cache data are retrieved in sequence from general purpose random access memory (i.e. 58 in Fig. 2) over common set of bus lines (i.e. 56 in Fig. 2 and set of bus lines made with combination of tag and data lines shown in Fig. 3; a single unified memory bus as disclosed in the Abstract) that connects the microprocessor (i.e. 52 in Fig. 2) to the cache memory bank (i.e. 58 in Fig. 2) (e.g. see Figs. 2-3 and the Abstract).

Neither BOI nor Feierbach teaches the further limitation of subsequent to retrieving the cache tag into the microprocessor, the cache data is retrieved into the microprocessor from the bank of the general purpose random access memory. Chen, on the other hand, teaches that first the address issued by the CPU (10 in Fig. 2) is compared with the tag address stored in the tag RAM (i.e. 30 in Fig. 2); and then if the result of the comparison is a cache hit, then the corresponding data is accessed from the data SRAM (i.e. 20 in Fig. 2) (e.g. see Figs. 2 and 4 and Col. 2, lines 18-34), in other words, the cache data is retrieved subsequent to retrieving the cache tag and these two retrieval processes do not overlap in time as claimed. Accordingly, it would

have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teachings of Chen in the method taught by the combination of BOI and Feierbach. In doing so, the data is retrieved from the data cache only if it exists in the data cache otherwise from the main memory. Therefore, the data traffic on the cache data/address bus is reduced by not receiving the wrong data. Therefore, the power saving and the performance of the system increases. Although Chen is not retrieving the cache tag in the microprocessor, it would have been obvious to retrieve it and compare it with the memory address requested by the microprocessor inside the microprocessor as taught by Feierbach for the benefits listed above.

As per claim 9, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above and furthermore, BOI teaches that the comparison circuitry identifies whether the memory address supplied by the microprocessor matches the data resident in the level 2 cache, which is similar to mapping the memory address into a cache tag address and a cache data address that are provided to the general purpose RAM to retrieve the cache tag and the cache data therefrom (e.g. see page 6, line 20 – page 7, line 3 and Fig. 4). Furthermore, as shown in Fig. 4 of BOI, the cache tag address and the cache data address are distinct from each other since

As per claims 10-12, see arguments with respect to the rejection of claims 3-4 and 7, respectively. Claims 10-12 are also rejected based on the rationale as the rejection of claims 3-4 and 7, respectively.

As per claim 26, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above and furthermore, BOI teaches that the address

transformation circuit (inherent) is configured to map a main memory space into a set of cache tag addresses and a set of cache data addresses, wherein the set of cache tag addresses and the set of cache data addresses are mutually exclusive such that cache tags and cache data may be stored in a common memory array (i.e. cache data are stored in the Level 2 cache data element in separate locations from the cache tags in the Level 2 cache tag element as shown in Fig. 4) (e.g. see Fig. 4).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Feierbach, further in view of Chen, further in view of Steely, Jr. et al. (USPN: 5,235,697) hereinafter, Steely.

As per claim 2, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above. However, none of them teaches that the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing the cache tag to the memory address. Steely, on the other hand, teaches that the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing the cache tag to the memory address (e.g. see Col. 4, lines 12-20). Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement the feature taught by Steely in the method taught by the combination of BOI, Feierbach and Chen so by performing parallel operations, it permits the CPU to immediately use the data from the predicted data RAM, before completion of the tag comparison but subject to later receipt of a mis-predict signal indicative of an incorrect prediction by the set prediction RAM. In other

words, in case if the cache tag does match with the memory address, i.e. cache hit, then the requested data is retrieved faster from the data RAM by performing the look-ahead step, i.e. starting the data retrieval step before finishing the tag compare step. In doing so, the data latency will be reduced and therefore, the overall performance of the microprocessor increases.

8. Claims 13-15, 17 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the BOI in view of Feierbach.

As per claim 13, BOI teaches a microprocessor (shown in Fig. 4) comprising a central processing unit (i.e. the CPU shown in Fig. 4) that supplies a memory address for performing a memory read operation. The further limitation of, having an address transformation circuit that converts/translates the memory address supplied by the central processing unit into a first address for retrieving a cache tag from an external cache memory and into a second address for retrieving cache data from the external cache memory, in inherently embedded in the microprocessor taught by BOI. The Fig. 4 of BOI clearly shows that the microprocessor provides the cache index (i.e. the cache memory address) to the cache data and tag memories (e.g. see Fig. 4). Therefore, there has to be an address transformation circuit present in the microprocessor taught by BOI to convert the memory address into the cache index (i.e. the cache memory address) for reading the cache tag and cache data from the cache memory bank.

However BOI does not teach the further limitation of having a comparison circuit that compares the memory address supplied by the central processing unit and the

cache tag retrieved from the external cache memory to assess whether said cache data is valid. Feierbach, on the other hand, teaches that the microprocessor (i.e. the CPU 52 in Fig. 2) performs the tag comparison (e.g. see Col. 4, line 56-59 and Fig. 2). Therefore, there has to be a comparison circuit inherently present in the microprocessor taught by Feierbach. Furthermore, the comparison of the cache tag with the memory address occurs within the microprocessor and in order to do that the cache tag has to be retrieved into the microprocessor as claimed. Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teachings of Feierbach in the method taught by BOI. In doing so, if a tag match occurs, then a cache hits exists and data *already* retrieved from the cache memory into the microprocessor can be processed. Therefore, the data latency reduces and the overall performance of the microprocessor increases. Also by doing so, any RAM memory can be used as tag RAM and the user can upgrade the system by replacing the tag RAM with the general purpose RAM without having the built-in comparison circuitry. Therefore, it would be cheaper to expand the tag RAM space.

As per claim 14, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, Feierbach also discloses "... external cache data is returned shortly after the address is launched ... [So] If a tag match occurs, then a cache hit exists and the data retrieved from the cache can be processed." (e.g. see Col. 4, line 39-55 and Fig. 5), i.e. the cache data is retrieved from the external cache memory while the cache tag comparison with the memory address is being performed into the microprocessor as claimed.

As per claim 15, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches about using the cache index (i.e. the combination of first and second addresses as claimed), i.e. using the second address to perform a sequence of memory read operations to retrieve said cache data from the external cache memory (e.g. see Fig. 4). Note: The BOI still reads on the claimed limitations since the cache index of BOI is the combination of both first and second addresses as claimed and claim 15 does not state specifically "only the second address".

As per claim 17, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that the address transformation circuit subdivides an addressable memory space of the external cache memory into a plurality of cache tag locations and a plurality of cache data locations (i.e. 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4).

As per claim 19, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that the microprocessor is configured to use a single bank of general purpose random access memory (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) as said external cache memory (e.g. see Fig. 4).

As per claim 20, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that the external cache memory (i.e. the combination of the Level 2 cache data element and the Level 2 cache tag element in Fig. 4) that stores both cache tags and cache data in separate memory

locations (i.e. cache data are stored in the Level 2 cache data element in separate locations from the cache tags in the Level 2 cache tag element) (e.g. see Fig. 4).

As per claim 21, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that the microprocessor uses the external cache memory as a level 2 cache (i.e. the combination of 'Level 2 Cache Data Element' and 'Level 2 Cache Tag Element' shown in Fig. 4) (e.g. see Fig. 4).

As per claim 22, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, Feierbach teaches that the microprocessor (i.e. 52 in Fig. 2) is configured to retrieve the cache tag and the cache data are retrieved from general purpose random access memory (i.e. 58 in Fig. 2) over common set of bus lines (i.e. 56 in Fig. 2 and set of bus lines made with combination of tag and data lines shown in Fig. 3; a single unified memory bus as disclosed in the Abstract) that connects the microprocessor (i.e. 52 in Fig. 2) to the cache memory bank (i.e. 58 in Fig. 2) (e.g. see Figs. 2-3).

As per claim 23, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches, as described above in the rejection of claim 13, a microprocessor (shown in Fig. 4) comprising a central processing unit (i.e. the CPU shown in Fig. 4) that supplies a memory address for performing a memory read operation (e.g. see Fig. 4). The further limitation of, having an address transformation circuit that converts/translates the memory address supplied by the central processing unit into a first address for retrieving a cache tag from an

external cache memory and into a second address for retrieving cache data from the external cache memory, in inherently embedded in the microprocessor taught by BOI. The Fig. 4 of BOI clearly shows that the microprocessor provides the cache index (i.e. the cache memory address) to the cache data and tag memories (e.g. see Fig. 4). Therefore, there has to be an address transformation circuit present in the microprocessor taught by BOI to convert the memory address into the cache index (i.e. the cache memory address) for reading the cache tag and cache data from the cache memory bank. In other words, the first transformation function and the second transformation function for generating the first and second addresses, respectively, as claimed are inherent in the BOI teachings. Note: Although the first and second addresses are same in the BOI prior art, it stills reads on the claimed limitations since the claim does not specify that the first and second addresses are different.

As per claim 24, the combination of BOI and Feierbach teaches the claimed invention as described above and furthermore, BOI teaches that the address transformation circuit (inherent) is configured to map a main memory space into a set of cache tag addresses and a set of cache data addresses, wherein the set of cache tag addresses and the set of cache data addresses are mutually exclusive such that cache tags and cache data may be stored in a common memory array (i.e. cache data are stored in the Level 2 cache data element in separate locations from the cache tags in the Level 2 cache tag element as shown in Fig. 4) (e.g. see Fig. 4).

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Feierbach, further in view of Vanka et al. (USPN: 5,699,540) hereinafter, Vanka.

As per claim 16, the combination of BOI and Feierbach teaches the claimed invention as described above, but failed to teach that the microprocessor is configured to abort said sequence of memory read operations when a comparison performed by the comparison circuit reveals that the cache data is not valid. Vanka, however, teaches that in the case where the cache data is not valid (i.e. the DRAM data to be accessed is invalid), the sequence of memory read operations are aborted (i.e. the CDC aborts the bus master access) (e.g. see Col. 5, lines 11-13). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Vanka in the microprocessor taught by the combination of BOI and Feierbach. In doing so, the data latency of the valid data is reduced by not waiting for remaining *invalid* data to be read then invalidating them and then reading the *valid* data from the main memory. Therefore, the performance of the microprocessor is increased.

10. Claims 18 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Feierbach, further in view of Gaskins et al. (USPN: 5,809,562) hereinafter, Gaskins.

As per claim 18, the combination of BOI and Feierbach teaches the claimed invention as described above, but failed to teach that the number of said cache data locations is approximately three times the number of said cache tag locations. Gaskins,

on the other hand, teaches that the number of said cache data locations (i.e. the sub cache line locations 214, 216, 218 and 220 in Fig. 2) is approximately three times the number of said cache tag locations (i.e. the tag lines 212 in Fig. 2) (e.g. see Fig. 2). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Gaskins in the microprocessor taught by the combination of BOI and Feierbach. In doing so, i.e. by not keeping the number of cache tag locations same as the number of cache data locations, the loss of extra cache space for storing one cache tag location per cache data location is avoided.

As per claim 25, the combination of BOI and Feierbach teaches the claimed invention as described above, but failed to teach that the set of cache data addresses is larger than the set of cache tag addresses. Gaskins, on the other hand, teaches that the number of said cache data locations (i.e. the sub cache line locations 214, 216, 218 and 220 in Fig. 2) is larger (approximately three times) than the number of said cache tag locations (i.e. the tag lines 212 in Fig. 2) (e.g. see Fig. 2). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Gaskins in the microprocessor taught by the combination of BOI and Feierbach. In doing so, i.e. by not keeping the number of cache tag locations same as the number of cache data locations, the loss of extra cache space for storing one cache tag location per cache data location is avoided.

11. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over BOI in view of Feierbach, further in view of Chen, further in view of Gaskins.

As per claim 27, the combination of BOI, Feierbach and Chen teaches the claimed invention as described above, however, none of them teaches that the set of cache data addresses is larger than the set of the cache tag addresses. Gaskins, on the other hand, teaches that the number of said cache data locations (i.e. the sub cache line locations 214, 216, 218 and 220 in Fig. 2) is larger (approximately three times) than the number of said cache tag locations (i.e. the tag lines 212 in Fig. 2) (e.g. see Fig. 2). Accordingly, it would have been obvious to one ordinary skilled in the art at the time of the current invention was made to implement the teaching of Gaskins in the microprocessor taught by the combination of BOI, Feierbach and Chen. In doing so, i.e. by not keeping the number of cache tag locations same as the number of cache data locations, the loss of extra cache space for storing one cache tag location per cache data location is avoided.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on M-F 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HBP
HBP

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100